WHAT IS CLAIMED AS NEW AND DESIRED TO BE PROTECTED BY LETTERS PATENTS IS:

1. A bonding method, comprising:

forming first and second bonding surfaces;

etching said first and second bonding surfaces; and

bonding together at room temperature said first and second bonding surfaces after said etching step.

2. A method as recited in claim 1, wherein said etching step comprises:

etching said first and second bonding surfaces such that respective surface roughnesses of said first and second bonding surfaces after said etching are substantially the same as respective surface roughnesses before said etching.

3. A method as recited in claim 2, comprising:

forming said first and second bonding surfaces to have a surface roughness in a range of 0.1 to 3.0 nm.

4. A method as recited in claim 1, wherein said etching step comprises:

activating said first and second bonding surfaces and forming selected bonding groups on said first and second bonding surfaces.

5. A method as recited in claim 4, comprising:

forming bonding groups capable of forming chemical bonds at approximately room temperature.

6. A method as recited in claim 1, comprising:

forming chemical bonds between said bonding surfaces allowing bonded groups to

diffuse or dissociate away from an interface of said first and second bonding surfaces.

7. A method as recited in claim 6, comprising:

increasing bonding strength between said first and second bonding surfaces by diffusing or dissociating away said bonding groups.

8. A method as recited in claim 1, wherein said etching step comprises:

forming a monolayer of one of a desired atom and a desired molecule on said bonding surface.

9. A method as recited in claim 8, wherein said etching step comprises:

forming a few monolayers of one of a desired atom and a desired molecule on said bonding surface.

10. A method as recited in claim 1, comprising:

after said etching step, immersing said first and second bonding surfaces in a solution to form bonding surfaces terminated with desired species.

11. A method as recited in claim 10, wherein said species comprise at least one of a silanol group, an NH_2 group, a fluorine group and an HF group.

12. A method as recited in claim 10, wherein said etching step comprises:

forming a monolayer of one of a desired atom and a desired molecule on said bonding surface.

13. A method as recited in claim 1, wherein said etching comprises:

exposing said first and second bonding surfaces to a plasma.

14. A method as recited in claim 1, comprising:

exposing said first and second bonding surfaces to one of an oxygen, argon, NH_3 and CF_4 plasma process.

15. A method as recited in claim 14, comprising:

conducting said plasma process in one of RIE mode, ICP mode, plasma mode and sputtering mode.

16. A method as recited in claim 1, comprising:

polishing respective first and second bonding surfaces to respective desired surface roughnesses and planarity; and

etching said first and second bonding surfaces after said polishing to activate said first and second bonding surfaces.

17. A method as recited in claim 16, wherein:

forming at least one of said first and second bonding surfaces comprises depositing a polishable material on a non-planar surface.

18. A method as recited in claim 17, wherein depositing said polishable material comprises depositing one of silicon oxide, silicon nitride or a dielectric polymer.

19. A method as recited in claim 1, wherein said etching step comprises:

increasing available bonding energy of bonding pairs on said first and second bonding surfaces at approximately room temperature.

20. A method as recited in claim 19, comprising:

obtaining a bond of at least 500 mJ/m^2.

21. A method as recited in claim 19, comprising:

obtaining a bond of at least 1000 mJ/m^2.

22. A method as recited in claim 19, comprising:

obtaining a bond of at least 2000 mJ/m^2.

23. A method as recited in claim 1, comprising:

forming a bond of at least 500 mJ/m^2.

24. A method as recited in claim 1, comprising:

obtaining a bond of at least 1000 mJ/m^2.

25. A method as recited in claim 1, comprising:

obtaining a bond of at least 2000 mJ/m^2.

26. A method as recited in claim 1, comprising:

forming chemical bonds between said bonding surfaces.

27. A method as recited in claim 26, comprising:

forming chemical bonds between said bonding surfaces in one of ambient and vacuum.

28. A method as recited in claim 26, comprising:

forming chemical bonds between said bonding surfaces in one of low and ultra high and vacuum.

29. A method as recited in claim 1, comprising:

forming a bond of sufficient energy to virtually eliminate wafer bowing during subsequent processing of said bonded bonding surfaces.

30. A method as recited in claim 29, comprising:

forming a bond of sufficient energy to virtually eliminate wafer bowing during subsequent thermal cycling of said bonded bonding surfaces.

31. A method as recited in claim 1, wherein said etching step comprises:

increasing available bonding energy of bonding pairs on said first and second bonding surfaces at approximately room temperature; and

propagating said bonding at room temperature.

32. A method as recited in claim 31, comprising:

propagating chemical bonding at room temperature.

33. A method as recited in claim 1, comprising:

depositing silicon dioxide as first and second bonding materials having said first and second bonding surfaces; and

etching said first and second bonding surfaces using an oxygen plasma.

34. A method as recited in claim 33, comprising:

rinsing said bonding materials in an ammonia-based solution after said etching.

35. A method as recited in claim 34, comprising:

rinsing said bonding materials in ammonium hydroxide after said etching.

36. A method as recited in claim 34, comprising:

rinsing said bonding materials in ammonium fluoride after said etching.

37. A method as recited in claim 1, comprising:

etching said first and second bonding surfaces under vacuum; and

bonding said first and second bonding surfaces without breaking said vacuum.

38. A method as recited in claim 1, comprising:

depositing a bonding material on each of first and second surfaces to obtain said first and second bonding surfaces.

39. A method as recited in claim 38, comprising:

depositing one of silicon dioxide and silicon nitride as said bonding material.

40. A method as recited in claim 1, comprising:

depositing silicon dioxide as said bonding material;

etching said silicon dioxide using one of oxygen, CF_4, and Ar plasma RIE; and

rinsing said silicon dioxide in an ammonia-based solution after said etching.

41. A method as recited in claim 1, comprising:

etching said first and second bonding materials using a wet etch process.

42. A method as recited in claim 42, comprising:

immersing said first and second bonding surfaces into a solution after said etching.

43. A method as recited in claim 1, comprising:

depositing silicon dioxide as said bonding material;

etching said silicon dioxide using one of diluted HF and diluted NH_4F.

44. A method as recited in claim 43, comprising:

rinsing said silicon dioxide in an ammonia-based solution after said etching.

45. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces as silicon; and

etching said bonding surfaces using a solution of HNO_3 and diluted HF.

46. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces as silicon each having a native oxide layer; and

activating said native oxide layer using said etching step.

47. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces each as silicon having a native oxide layer; and

exposing said first and second bonding surfaces to an oxygen plasma to etch said native oxide layers.

48. A method as recited in claim 47,

creating a defective zone in said silicon during plasma etching.

49. A method as recited in claim 1, comprising:

etching said first and second bonding materials using a plasma RIE process;

forming a region having defects proximate to said bonding surface; and

removing bonding by-products using said region.

50. A method as recited in claim 1, wherein said etching comprises:

activating said first and second bonding surfaces; and

creating a region under said first and second bonding surfaces for removing bonding by-products.

51. A method as recited in claim 1, comprising:

creating a region proximate to said first and second bonding surfaces for at least one of removal and conversion of bonding by-products to a species capable of being absorbed by or diffusing away from said bonding surfaces.

52. A method as recited in claim 1, comprising:

forming said first bonding surface by depositing an oxide layer on a first semiconductor wafer;

forming said second bonding surface by depositing an oxide layer on a second semiconductor wafer; and

bonding said first and second semiconductor wafers.

53. A method as recited in claim 1, comprising:

forming said first bonding surface as a deposited oxide layer on a first semiconductor wafer, said first wafer comprising a first substrate and a first active region;

forming said second bonding surface as a deposited oxide layer on a second

semiconductor wafer, said second wafer comprising a second substrate and a second active region;

bonding said first and second semiconductor wafers; and

removing at least a substantial portion of one of said first and second substrates after said bonding.

54. A method as recited in claim 1, comprising:

forming said first bonding surface as a deposited oxide layer on a semiconductor wafer, said wafer comprising a substrate and an active region;

forming said second bonding surface as a surrogate substrate;

bonding said wafer and said surrogate substrate; and

removing at least a substantial portion of said first substrate after said bonding.

55. A method as recited in claim 1, wherein said bonding comprises:

maintaining contact between said first and second bonding surfaces for a specified period to produce bonding polymerization and allow removal of by-products.

56. A method as recited in claim 55, comprising:

maintaining said contact between said first and second bonding surfaces for a period less than about 20 hours.

57. A method as recited in claim 1, wherein said bonding comprises:

maintaining said first and second bonding surfaces for a specified period in ambient to remove bonding by-products.

58. A method as recited in claim 1, comprising:

etching said first and second bonding surfaces using a bonding fixture under vacuum;

bonding said first and second bonding surfaces using said fixture to bring together

said first and second bonding surfaces while maintaining said vacuum.

59. A method as recited in claim 1, comprising:

forming a first oxide layer on a first wafer containing electrical devices; and

polishing said first oxide layer to form said first bonding surface.

60. A method as recited in claim 59, comprising:

forming a second oxide layer on a second wafer containing electrical devices; and

polishing said second oxide layer to form said second bonding surface.

61. A method as recited in claim 60, comprising:

forming said first oxide layer on said first wafer containing electrical devices of a first technology; and

forming said second oxide layer on said second wafer containing electrical devices of a second technology different from said first technology.

62. A method as recited in claim 60, comprising:

interconnecting said first and second devices.

63. A method as recited in claim 60, comprising:

forming said first bonding surface on a surface of a one of a thermal spreader, surrogate substrate, antenna, wiring layer, and pre-formed multi-layer interconnect.

64. A method as recited in claim 60, comprising:

forming said second bonding surface on a surface of a one of a thermal spreader, surrogate substrate, antenna, wiring layer, and pre-formed multi-layer interconnect.

65. A method as recited in claim 1, comprising:

forming said first bonding surface on a first wafer containing a first integrated circuit.

66. A method as recited in claim 65, comprising:

forming said second bonding surface on a second wafer containing a second integrated circuit.

67. A method as recited in claim 66, comprising:

forming said first bonding surface on said first wafer containing said first integrated circuit of a first technology; and

forming said second bonding surface on said second wafer containing said second integrated circuit of a second technology different from said first technology.

68. A method as recited in claim 66, comprising:

interconnecting said first and second integrated circuits.

69. A method as recited in claim 1, comprising:

said first and second bonding surfaces being substantially planar.

70. A method as recited in claim 1, wherein:

forming said first and second bonding surfaces comprises depositing a dielectric material.

71. A method as recited in claim 70, comprising:

polishing said dielectric material to a desired planarity and surface roughness.

72. A method as recited in claim 70, comprising:

depositing said dielectric material on a non-planar surface.

73. A method as recited in claim 72, wherein:

said polishing comprises chemical-mechanical polishing.

74. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces to be non-planar; and

polishing said first and second bonding surfaces to a desired planarity and surface

roughness.

75. A method as recited in claim 74, wherein:

said polishing comprises chemical-mechanical polishing.

76. A method as recited in claim 1, where said etching comprises:

activating said bonding surfaces; and

terminating said bonding surfaces with a desired species.

77. A method as recited in claim 1, wherein said etching comprises:

a first etching step to activate said bonding surfaces; and

a second etching step to terminate said bonding surfaces with a desired species.

78. A method as recited in claim 1, comprising:

obtaining etched bonding surfaces using said etching step; and

exposing said bonding surfaces to a gaseous chemical environment to terminate said etched bonding surfaces with a desired species.

79. A method as recited in claim 1, comprising:

forming a first oxide layer on a first wafer containing electrical devices and having a non-planar surface; and

forming a second oxide layer on a second wafer containing electrical devices; and

polishing said first and second oxide layers to form said first and second bonding surfaces, respectively.

80. A method as recited in claim 79, comprising:

forming said second oxide layer on said second wafer having a non-planar surface.

81. A method as recited in claim 1, comprising:

forming a first oxide layer on a first wafer containing electrical devices and having an

irregular surface topology; and

forming a second oxide layer on a second wafer containing electrical devices; and

polishing said first and second oxide layers to form said first and second bonding surfaces, respectively.

82. A method as recited in claim 81, comprising:

forming said second oxide layer on said second wafer having an irregular surface topology.

83. A bonding method, comprising:

forming first and second bonding surfaces each having a surface roughness in a range of 0.1 to 3 nm;

removing material from said first and second bonding surfaces while maintaining said surface roughness; and

directly bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 500 mJ/m^2.

84. A method as recited in claim 83, comprising:

directly bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 1000 mJ/m^2.

85. A method as recited in claim 83, comprising:

directly bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 2000 mJ/m^2.

86. A method as recited in claim 83, comprising:

activating said first and second bonding surfaces and forming selected bonding groups on said first and second bonding surfaces.

87. A method as recited in claim 83, comprising:

polishing respective first and second bonding surfaces to said surface roughness; and

etching said first and second bonding surfaces after said polishing to activate said first and second bonding surfaces.

88. A method as recited in claim 83, comprising:

converting bonding by-products to a species capable of being absorbed by or diffusing away from said bonding surfaces during said bonding step.

89. A method as recited in claim 83, comprising:

etching said first and second bonding surfaces using a plasma RIE process;

forming a subsurface layer having defects; and

removing bonding by-products using said subsurface layer.

90. A method as recited in claim 83, comprising:

forming said first bonding surface as a surface of a first semiconductor wafer having devices formed therein; and

forming said second bonding surface as a surface of a second semiconductor wafer having devices formed therein.

91. A method as recited in claim 90, wherein one of said first and second wafers comprises a substrate, said method comprising:

removing a substantial portion of said one of said first and second wafers.

92. A method as recited in claim 90, comprising:

interconnecting devices in said first and second wafers.

93. A method as recited in claim 83, comprising:

forming a first insulating layer on a first wafer containing electrical devices;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices; and

polishing said second oxide layer to form said second bonding surface.

94. A method as recited in claim 83, comprising:

forming a first insulating layer on a first wafer containing electrical devices and having an irregular surface topology;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices and having an irregular surface topology; and

polishing said second oxide layer to form said second bonding surface.

95. A bonding method, comprising:

forming first and second bonding surfaces;

etching said first and second bonding surfaces;

terminating said first and second bonding surfaces with a species allowing formation of chemical bonds at about room temperature; and

bonding said first and second bonding surfaces at about room temperature.

96. A method as recited in claim 95, comprising:

bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 500 mJ/m^2.

97. A method as recited in claim 95, comprising:

bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 1000 mJ/m^2.

98. A method as recited in claim 95, comprising:

bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 2000 mJ/m^2.

99. A method as recited in claim 95, comprising:

activating said first and second bonding surfaces prior to said bonding step.

100. A method as recited in claim 95, comprising:

polishing said first and second bonding surfaces; and

etching said first and second bonding surfaces after said polishing to activate said first and second bonding surfaces.

101. A method as recited in claim 95, comprising:

converting bonding by-products to a species capable of being absorbed by or diffusing away from said bonding surfaces during said bonding step.

102. A method as recited in claim 95, comprising:

forming said first bonding surface as a surface of a first semiconductor wafer having devices formed therein; and

forming said second bonding surface as a surface of a second semiconductor wafer having devices formed therein.

103. A method as recited in claim 102, wherein one of said first and second wafers comprises a substrate, said method comprising:

removing a substantial portion of said one of said first and second wafers.

104. A method as recited in claim 102, comprising:

interconnecting devices in said first and second wafers.

105. A method as recited in claim 95, comprising:

forming a first insulating layer on a first wafer containing electrical devices;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices; and

polishing said second oxide layer to form said second bonding surface.

106. A method as recited in claim 95, comprising:

forming a first insulating layer on a first wafer containing electrical devices and having an irregular surface topology;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices and having an irregular surface topology; and

polishing said second oxide layer to form said second bonding surface.

107. A bonded device, comprising:

a first material having a first etched bonding surface; and

a second material having a second etched bonding surface directly bonded to said first bonding surface at room temperature having a bonding strength of at least 500 to 2000 mJ/m^2.

108. A device as recited in claim 107, comprising:

said first and second bonding surfaces being activated and terminated with a desired bonding species.

109. A device as recited in claim 108, wherein said desired species comprise:

a monolayer of one of a desired atom and a desired molecule on said bonding surface.

110. A device as recited in claim 108, wherein said desired species comprise at least

one of a silanol group, an NH_2 group, a fluorine group and an HF group.

111. A device as recited in claim 107, comprising:

said first and second bonding surfaces each having a defective region located proximate to said first and second bonding surfaces, respectively.

112. A device as recited in claim 107, wherein:

said first material comprises a surface of a first semiconductor wafer having devices formed therein; and

said second material comprises a surface of a second semiconductor wafer having devices formed therein.

113. A device as recited in claim 112, wherein one of said first and second wafers comprises a device region after removing a substantial portion of a substrate of said one of said first and second wafers.

114. A device as recited in claim 112, comprising:

devices in said first and second wafers being interconnected.

115. A device as recited in claim 112, comprising:

said first and second wafers being different technologies.

116. A device as recited in claim 107, wherein:

one of said first and second wafers comprises an integrated circuit.

117. A device as recited in claim 116, comprising:

devices in said first and second wafers being interconnected.

118. A device as recited in claim 116, comprising:

said first and second wafers having an irregular surface topology.

119. A device as recited in claim 107, wherein:

said first material comprises a first wafer containing electrical devices and having a first non-planar surface; and

said first bonding surface comprises a polished and etched deposited oxide layer on said first non-planar surface.

120. A device as recited in claim 119, wherein:

said second material comprises a second wafer containing electrical devices and having a second non-planar surface; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second non-planar surface.

121. A method as recited in claim 107, wherein:

said first material comprises a first wafer containing electrical devices and having a first surface with irregular topology; and

said first bonding surface comprises a polished, planarized and etched deposited oxide layer on said first surface.

122. A method as recited in claim 121, comprising:

said second material comprises a second wafer containing electrical devices and having a second surface with irregular topology; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second surface.

123. A bonded device, comprising:

a first material having a first etched and activated bonding surface terminated with a first desired bonding species; and

a second material having a second etched and activated bonding surface terminated

with a second desired bonding species bonded to said first bonding surface at room temperature.

124. A device as recited in claim 123, wherein said species comprise at least one of a silanol group, an NH_2 group, a fluorine group and an HF group.

125. A device as recited in claim 123, comprising:

said first and second bonding surfaces each having a defective region located proximate to said surfaces.

126. A device as recited in claim 123, wherein said desired species comprises:

a monolayer of one of a desired atom and a desired molecule on said bonding surface.

127. A device as recited in claim 123, comprising:

said second bonding surface bonded to said first bonding surface at room temperature having a bonding strength of at least 500 to 2000 mJ/m^2.

128. A device as recited in claim 123, wherein:

said first bonding surface comprises a surface of a first semiconductor wafer having devices formed therein; and

said second bonding surface comprises a surface of a second semiconductor wafer having devices formed therein.

129. A device as recited in claim 123, wherein one of said first and second wafers comprises a device region after removing a substantial portion of a substrate of said one of said first and second wafers.

130. A device as recited in claim 123, comprising:

devices in said first and second wafers being interconnected.

131. A device as recited in claim 123, comprising:

said first and second wafers being different technologies.

132. A device as recited in claim 123, wherein:

one of said first and second wafers comprises an integrated circuit.

133. A device as recited in claim 123, comprising:

devices in said first and second wafers being interconnected.

134. A device as recited in claim 123, wherein:

said first material comprises a first wafer containing electrical devices and having a first non-planar surface; and

said first bonding surface comprises a polished and etched deposited oxide layer on said first non-planar surface.

135. A device as recited in claim 134, wherein:

said second material comprises a second wafer containing electrical devices and having a second non-planar surface; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second non-planar surface.

136. A method as recited in claim 123, wherein:

said first material comprises a first wafer containing electrical devices and having a first surface with irregular topology; and

said first bonding surface comprises a polished, planarized and etched deposited oxide layer on said first surface.

137. A method as recited in claim 123. wherein:

said second material comprises a second wafer containing electrical devices and having a second surface with irregular topology; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second surface.